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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/525,862	02/25/2005	Remco Cornelis Herman Van De Beek	NL02 0803 US	2188

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EXAMINER	
JAGER, RYAN C	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 06/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/525,862	VAN DE BEEK ET AL.	
	Examiner	Art Unit	
	Ryan C. Jager	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☒ Claim(s) *7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 February 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities:

The reference number 113 is referred to as both a "binary divider" and a "frequency divider" on page 7, paragraph 1 of the specification. To be a binary divider the block would need two inputs which is not shown in figure 5, disclosing block 113. For the purposes of this action, 113 of figure 5 is assumed to be a frequency divider.

Also, it is suggested the recitation "The splitter 103" on line 6 be changed to --The frequency divider 113--.

It is suggested the recitation "inverter 110" on page 7 lines 14-15 be changed to --inverter 111--.

Appropriate correction is required.

Claim Objections

2. Claims 1, 2, 3 and 6 are objected to because of the following informalities:

With respect to claim 1, the recitations "mutually phase shifted signals" on line 2 and "relative phase shifted signals" on line 6 are referring to the same signals. The recitation of "mutually" should be changed to --relative-- on line 2 or "relative" changed to --mutually-- on line 6.

The recitation of "relative phase shifted signals" also occurs in claims 2, 3 and 6 and should be consistent with claim 1.

Claims 2-7 are objected to because they contain the objected to subject matter of claim 1.

With respect to claim 2, it is suggested the recitation "the first charge pump" be changed to --a first charge pump--.

Also in claim 2, it is suggested the recitation "the low-pass filter" be changed to --a low-pass filter--.

With respect to claim 3, line 2 recites "a signal generated by the voltage controlled oscillator" it is suggested this be changed to "the input signal generated by the voltage controlled oscillator" recited in claim 2 line 2-3.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 3 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With respect to claim 3, the recitation of "binary divider" is indefinite because a binary divider requires two inputs to divide, multiple inputs are not disclosed in the specification, drawings, or claims.

Claim 5 is misdescriptive, a quadrature voltage controlled oscillator acts as both the oscillator and the splitter. There would be no reason for an additional phase splitter to make the relative phase shifted signals in quadrature because the quadrature oscillator outputs quadrature signals.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1 and 2 are rejected under 35 U.S.C. 102(b) as being anticipated by Atkinson (UK Patent Application, GB, 2253316).

With respect to claim 1, figure 4 of Atkinson discloses, a phase locked loop (page 1 lines 3-5) comprising a phase detector for determining a phase difference between a reference signal (i/p 2) and mutually phase shifted signals (i and q) to generate frequency control signals (output of A and B) the phase detector comprising: means for obtaining a first one (output of B) of said frequency control signals by binary multiplication (output of A) of the reference signal (i/p 2) and one of the relative phase shifted signals (q); and means for obtaining a second one of said frequency control signals by binary multiplication (output of B) of the relative phase shifted signals (i and q).

With respect to claim 2, figure 4 of Atkinson discloses, a phase locked loop as claimed in claim 1, further comprising a splitter (13) for generating the relative phase shifted signals (i and q) the splitter having an input signal (i/p 1) generated by a voltage controlled oscillator coupled to the first charge pump (I1 and I2) and to the low-pass filter (C).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 3 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takeshita et al. (US Patent Application Publication 20020053950) in view of Atkinson (UK Patent Application, GB, 2253316) and further in view of Nakamura (USP 6072370)

With respect to claim 3, figure 1 of Takeshita et al. discloses the use of a frequency divider followed by a phase splitter, providing feedback in a PLL to a phase detector. Takeshita does not disclose a phase detector providing control signals by binary multiplication or a splitter comprising a divide by two circuit with first and second bi-stable circuits. However, figure 4 of Atkinson discloses a phase detector performing binary multiplication of mutually phase shifted signals and a reference signal to produce frequency control signals to a charge pump. Therefore it would have been obvious to one skilled in the art at the time the invention was made to modify the PLL in figure 1 of Takeshita et al. by replacing the phase detector (11, figure 1) of Takeshita et al with the phase detector (A and B) in figure 4 of Atkinson for the purpose of eliminating the need for producing a third phase shifted signal in the splitter and reducing the number of electronic components used in the circuit.

Further, the above combination teaches the use of a frequency divider followed by a phase splitter, providing feedback in a PLL to a phase detector performing binary

multiplication of mutally phase shifted signals and a reference signal to produce frequency control signals to a charge pump. But the above modification does not disclose a divide by two circuit with first and second bi-stable circuits. However, figure 7 of Nakamura discloses a divide-by-two circuit comprising a first and second bi-stable circuit for providing relative phase shifted feed back signals in a PLL. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to replace the phase splitter (176) in figure 1 of Takeshita et al. with the splitter in figure 7 of Nakamura for the purpose of reducing the size of the splitter circuit used in the PLL.

With respect to claim 6, the above modification discloses a phase locked loop as claimed in claim 1, further comprising a frequency detector (12) coupled to receive the reference signal (DATA) and the relative phase shifted signals (ICLK,QCLK) for supplying an up frequency detector signal (UP) and a down frequency detector signal (DOWN) to a first charge pump (14) coupled to the loop filter (C11).

6. Claims 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Atkinson (UK Patent Application, GB, 2253316) in view of Dalmia (USP 6683930, filed 12/23/99)

With respect to claim 4, figure 4 of Atkinson discloses all the limitations of this claim except the splitter comprises a series coupling of a delay line and an inverter. However, figure 6 of Dalmia discloses a signal splitter comprising a delay line (300a-b) in series with an inverter (300c) (column 4 discloses a delay line of inverters capable of producing different desired phases of an input signal by adding more inverters). Therefore it would have been obvious to one skilled in the art at the time the invention

was made to use a delay line of inverters to produce the desired phases of the input signal as output.

7. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Atkinson in view of Dalmia (USP 6683930).

Insofar as understood with respect to claim 5, figure 4 of Atkinson discloses all the limitations of this claim except for a quadrature oscillator providing the relative phase shifted signals. However, figures 4 and 6 of Dalmia disclose the use of a quadrature oscillator capable of producing the relative phase shifted signals in quadrature for feedback in a PLL. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to replace the oscillator in the PLL of Atkinson with a quadrature oscillator for the purpose of eliminating the need for the splitter (13) and therefore making the circuit smaller.

Allowable Subject Matter

Claim 7 would be allowable over the prior art of record if rewritten in independent form including all of the limitations of the base claim and any intervening claims because the latter, either alone or in combination, does not disclose nor render obvious a the specific frequency detector described in claim 7, in combination with the rest of the claimed limitations.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan C. Jager whose telephone number is (571) 272-7016. The examiner can normally be reached on M-F 8 am - 5 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

RCJ

Ryan C. Jager
5/18/2006

LONG NGUYEN
PRIMARY EXAMINER